REMARKS

Claims 1-22 were pending in this application and were each rejected. Claims 1-22 remain pending.

Reconsideration and full allowance of Claims 1-22 is respectfully requested.

I. REJECTION UNDER 35 U.S.C. § 103

The Office Action rejects Claims 1-22 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,761,469 to Greenley et al. ("Greenley") in view of McGreer, Brayton, Sangiovanni-Vincentelli, and Sahni's "Performance Enhancement through the Generalized Bypass Transform" from IEEE (c) 1991 ("McGreer"). The Applicant respectfully traverses this rejection.

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. (*MPEP § 2142; In re Fritch, 972 F.2d 1260, 1262, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992)*). The initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention is always upon the Patent Office. (*MPEP § 2142; In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Piasecki, 745 F.2d 1468, 1472, 223 U.S.P.Q. 785, 788 (Fed. Cir. 1984)*). Only when a *prima facie* case of obviousness is established does the burden shift to the Applicant to produce evidence of nonobviousness. (*MPEP § 2142; In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Rijckaert, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993)*). If the Patent Office does not produce a *prima facie* case of unpatentability,

then without more the Applicant is entitled to grant of a patent. (*In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Grabiak, 769 F.2d 729, 733, 226 U.S.P.Q. 870, 873 (Fed. Cir. 1985)*).

A *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. (*In re Bell, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993)*). To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed invention and the reasonable expectation of success must both be found in the prior art, and not based on the Applicant's disclosure. (*MPEP § 2142*).

Claims 1 and 14 recite a "load store unit" capable of transferring a first data value from a "data cache" to a "target one of [a] plurality of registers" during execution of a load operation. Claims 1 and 14 also recite a "shifter circuit" capable of shifting, sign extending, or zero extending the first data value "prior to loading [the] first data value into [the] target register." In addition, Claims 1 and 14 recite "bypass circuitry" capable of "transferring [the] first data value from [the] data cache directly to [the] target register without processing [the] first data value in [the] shifter circuit."

Claims 1 and 14 are crystal clear – the "shifter circuit" can process a data value before the data value is loaded from a data cache into a target register. Also, the "bypass circuitry" can transfer the data value from the data cache directly to the target register without the data value being processed by the "shifter circuit" (thereby bypassing the shifter circuit).

Greenley fails to disclose, teach, or suggest a structure that allows a data value to be transferred either (i) from a data cache to a target register through a shifter circuit, or (ii) directly from the data cache to the target register while bypassing the shifter circuit, as conceded in the Office Action.

In *Greenley*, all data passes from the data cache 180 through the aligning unit 170 and the sign extension unit 160 into the register files 150. Because of this, *Greenley* recites that all data passes through a shifter. More specifically, *Greenley* recites that all data passes through a shifter (the alignment unit 170 and/or the sign extension unit 160) before the data is stored in a register file 150.

McGreer discusses a mathematical model for a "generalized bypass transform" that "accelerate[s] circuits not by reducing path length but by making paths false." (Abstract). *McGreer* experiments using ripple-carry adders and carry-skip adders. *McGreer* does not teach anything about using bypass circuitry in an instruction execution pipeline of a data processor as recited in Claims 1 and 14. *McGreer* also does not teach doing anything in response to a determination that a pending instruction is a load word operation as recited in Claim 10. As such, *McGreer* fails to teach the limitations of the claims not taught by *Greenley*.

To the extent that *McGreer* teaches "bypass circuitry" at all, there is no teaching or suggestion that it would be operable in the context of the claimed invention or in the system of *Greenley*. It does not even appear to be analogous art.

Moreover, there is no motivation at all to combine these references. The Office Action's stated motivation is "to improve system performance." However, nothing in *Greenley* teaches or suggests that bypassing anything would improve performance. Similarly, nothing in *McGreer* teaches or suggests that its "generalized bypass transform" would improve performance at all in a pipelined processor by transferring data from a data cache to a target register, which is far different from the adders used in *McGreer*. In fact, *McGreer* specifically teaches away from any general application of this experimental model:

> Readers are cautioned that these results should be viewed in context; both the delay and area model used here are somewhat primitive, and hence these results should not be used to compare the proposed technique to others. We view these results as preliminary indications that the proposed technique may be of great value as a performance-enhancing transformation on combinational logic circuits. (page 187, col. 1, next-to-last paragraph.)

McGreer therefore both limits its teachings to combinational logic circuits and disclaims any general applicability. As such, there can be no motivation for one of skill in the art to first extend *McGreer's* teachings into another field of art, then modify them, then combine them into

Greenley's system for a purpose not considered by either *McGreer* or *Greenley*. The only relevance of *McGreer* at all appears to be that it includes the word "bypass."

Therefore, no cited reference or combinations of references discloses, teaches, or suggests a structure where a data value can either be (i) transferred from a data cache to a target register through a shifter circuit, or (ii) directly transferred from the data cache to the target register (while bypassing the shifter circuit).

For these reasons, the Office Action has not established a *prima facie* case of obviousness against Claims 1, 10, and 14 (and their dependent claims). Accordingly, the Applicant respectfully requests withdrawal of the § 103 rejection and full allowance of Claims 1-22.

II. CONCLUSION

The Applicant respectfully asserts that all pending claims in this application are in condition for allowance and respectfully requests full allowance of the claims.

SUMMARY

If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at *wmunck@davismunck.com*.

The Commissioner is hereby authorized to charge any additional fees connected with this communication (including any extension of time fees) or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

DAVIS MUNCK, P.C.

Date: Dec. 29, 2005

William A. Munck
Registration No. 39,308

P.O. Box 802432
Dallas, Texas 75380
Phone: (972) 628-3600
Fax: (972) 628-3616
E-mail: *wmunck@davismunck.com*